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## Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals

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Received: 19 August 2015  
Accepted: 02 December 2015  
Published: 08 January 2016

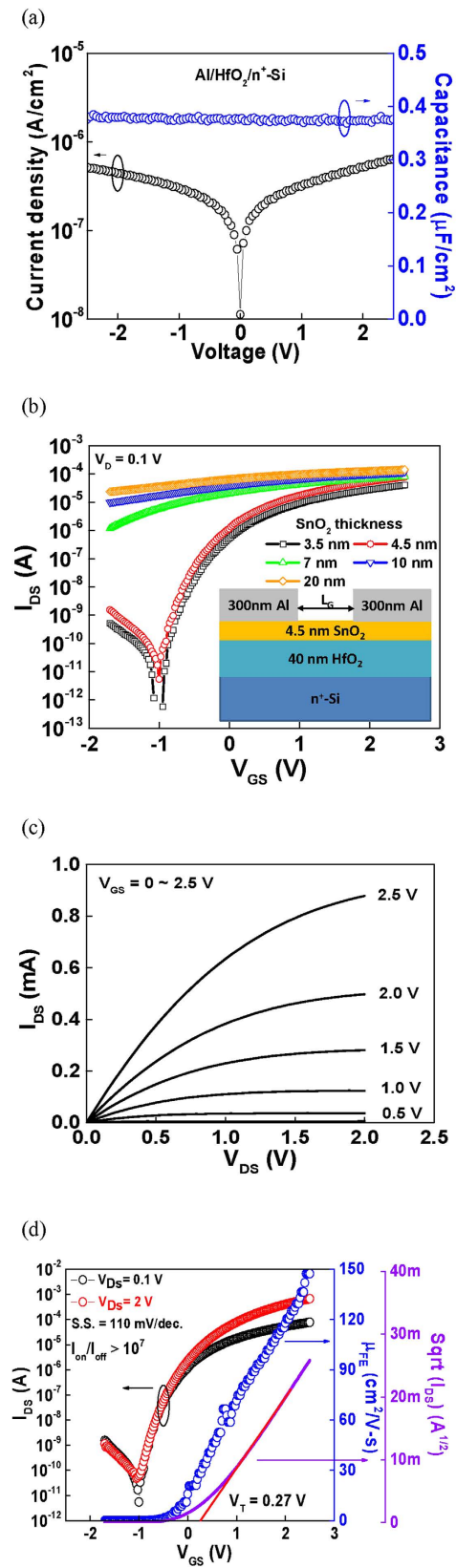
High mobility channel thin-film-transistor (TFT) is crucial for both display and future generation integrated circuit. We report a new metal-oxide TFT that has an ultra-thin 4.5 nm SnO<sub>2</sub> thickness for both active channel and source-drain regions, very high 147 cm<sup>2</sup>/Vs field-effect mobility, high  $I_{ON}/I_{OFF}$  of  $2.3 \times 10^7$ , small 110 mV/dec sub-threshold slope, and a low  $V_D$  of 2.5V for low power operation. This mobility is already better than chemical-vapor-deposition grown multi-layers MoS<sub>2</sub> TFT. From first principle quantum-mechanical calculation, the high mobility TFT is due to strongly overlapped orbitals.

The metal-oxide thin-film transistor (TFT)<sup>1–20</sup> is a revolutionary technology for displays due to its high mobility and simple process. The high mobility of zinc-oxide (ZnO)-based materials was attributed to the spatially spread metal ns orbitals with isotropic shape, which is possible to overlap the neighboring metal ns orbitals<sup>7</sup>. However, the high performance ZnO-based TFTs of InGaZnO<sup>7</sup>, bi-layer InSnO/InGaZnO<sup>11</sup>, InZnO<sup>13</sup>, and GaZnON<sup>18</sup> compounds usually contain Indium (In) or Gallium (Ga), which are rare elements in earth's crust. In addition, device performance is sensitive to the moisture degradation and atomic composition of these compound. Alternatively, high mobility, high transistor on-current ( $I_{ON}$ ), and low off-current ( $I_{OFF}$ ) TFTs are found in two-dimensional metal-chalcogenide<sup>21–28</sup>. However, chemical vapor deposition (CVD)-grown MoS<sub>2</sub><sup>25–28</sup> shows a considerably lower mobility compared with peeled-off flakes from crystals<sup>21–28</sup>. To further increase the display pixel density and drive organic light-emitting diodes (OLED), higher mobility and  $I_{ON}$  than those of ZnO-based TFTs are needed. The low DC and switching power consumptions are other technological trends for displays that require a low  $I_{OFF}$  and low operation voltage. In this study, a remarkably high field-effect mobility ( $\mu_{FE}$ ) of 147 cm<sup>2</sup>/Vs was demonstrated experimentally in tin-oxide (SnO<sub>2</sub>) TFT. This TFT also showed a high  $I_{ON}/I_{OFF}$  of  $2.3 \times 10^7$ , low sub-threshold swing (SS) of 0.11 V/decade, low threshold voltage ( $V_T$ ) of 0.27 V, low drive voltage of 2.5 V for low switching power, and ultra-thin layer with a thickness of 4.5 nm. Such ultra-thin thickness is comparable with that of multilayered MoS<sub>2</sub><sup>27</sup> for low DC standby power consumption. Notably, Sn (Group IV) has ns<sup>2</sup>np<sup>2</sup> electron configuration and directive sp<sup>3</sup> orbitals, which differ from those of Zn<sup>7</sup>. According to first principle quantum-mechanical calculations, the considerably high  $\mu_{FE}$  in SnO<sub>2</sub> TFT is caused by its overlapped s-orbitals even in an ns<sup>2</sup>np<sup>2</sup> configuration.

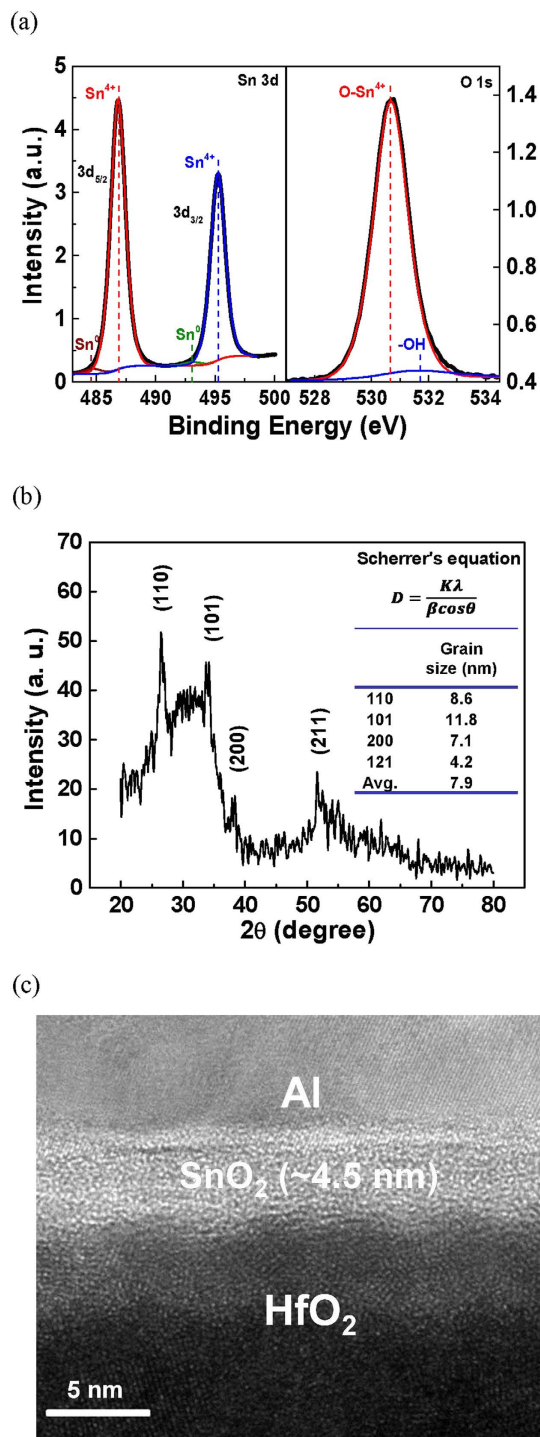
### Results

To increase the transistor  $I_{ON}$  and reduce the operation voltage, a high-dielectric-constant (high- $\kappa$ ) gate insulator<sup>12,15</sup> was used for the TFT. Figure 1(a) shows the current-voltage ( $I$ - $V$ ) and capacitance-voltage ( $C$ - $V$ ) characteristics of a gate capacitor with top Aluminum (Al) electrode, high- $\kappa$  hafnium-oxide (HfO<sub>2</sub>), and bottom n<sup>+</sup>-Si. In the Al/HfO<sub>2</sub>/n<sup>+</sup>-Si capacitor, a small leakage current of  $5.7 \times 10^{-7}$  A/cm<sup>2</sup> at 2 V was obtained at a capacitance density of 0.38  $\mu$ F/cm<sup>2</sup>. The high capacitance density yielded a low equivalent-oxide-thickness (EOT) of only 9.1 nm, which was due to the high- $\kappa$  HfO<sub>2</sub> with a  $\kappa$  of 17. Figure 1(b) shows the transistor's drain current versus gate voltage ( $I_{DS}$ - $V_{GS}$ ) characteristics of the SnO<sub>2</sub>/HfO<sub>2</sub> TFTs with 4.5 ~ 20 nm thick SnO<sub>2</sub>. The device with thick 20 nm SnO<sub>2</sub> failed to show proper pinch off  $I_{OFF}$  due to very high conductivity, although the device has very high  $I_{ON}$ . The device with 4.5 nm thick SnO<sub>2</sub> shows the best  $I_{ON}/I_{OFF}$  performance. Figure 1(c,d) show the transistor's drain current versus drain voltage ( $I_{DS}$ - $V_{DS}$ ),  $I_{DS}$ - $V_{GS}$ , and  $\mu_{FE}$ - $V_{GS}$  characteristics of the SnO<sub>2</sub>/HfO<sub>2</sub> TFT with 4.5 nm thick SnO<sub>2</sub>, respectively. The device was operated in the enhancement mode of an n-channel metal-oxide-semiconductor field-effect transistor (nMOSFET) at a low operation voltage of 2.5 V. The device also showed a high  $I_{ON}/I_{OFF}$  of  $2.3 \times 10^7$ , low SS of 110 mV/decade, and low  $V_T$  of 0.27 V. The  $V_T$  was extracted from the intercept of the linear  $I_{DS}^{1/2}$ - $V_{GS}$  curve in a saturation region. A high  $I_{ON}$  is crucial to drive the OLED and increase the display pixel density, whereas a

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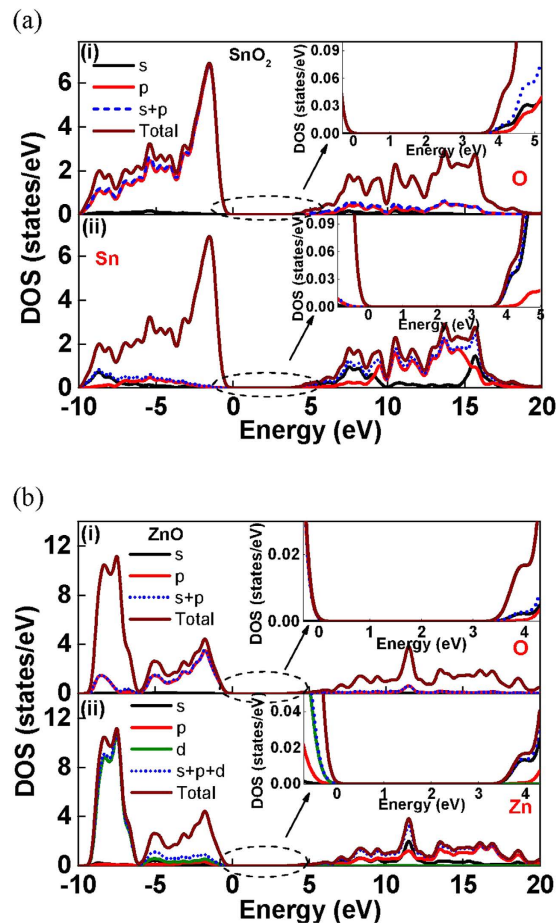


**Figure 1.** (a) *I*-*V* and *C*-*V* characteristics of gate capacitor, (b) *I*<sub>DS</sub>-*V*<sub>GS</sub> characteristics of Al/SnO<sub>2</sub>/HfO<sub>2</sub>/n<sup>+</sup>-Si TFTs with 20 ~ 3.5 nm SnO<sub>2</sub> layers, (c) *I*<sub>DS</sub>-*V*<sub>DS</sub> and (d) *I*<sub>DS</sub>-*V*<sub>GS</sub>, μ<sub>FE</sub>-*V*<sub>GS</sub> and Sqrt(*I*<sub>DS</sub>)-*V*<sub>GS</sub> characteristics of Al/SnO<sub>2</sub>/HfO<sub>2</sub>/n<sup>+</sup>-Si TFTs at 4.5 nm SnO<sub>2</sub> thickness. The gate length is 50 μm.



**Figure 2.** (a) XPS, (b) XRD, and (c) TEM analysis of SnO<sub>2</sub> formed on HfO<sub>2</sub>/n<sup>+</sup>-Si. The SnO<sub>2</sub> thickness is 20 nm for XPS and XRD analysis, while 4.5 nm for TEM.

low  $I_{OFF}$  is required to reduce the DC standby power. The low SS with the mean value and standard deviation of  $100.2 \pm 19.4$  mV/decade indicates the good oxide/semiconductor interface to turn on the transistor fast. The  $I_{ON}$  showed an inversely proportional relation with gate length in a wide gate length TFT, a typical method to extract mobility correctly for Si MOSFET and metal-gate/high- $\kappa$  MOSFET<sup>29–31</sup>. A remarkably high  $\mu_{FE}$  of 147 cm<sup>2</sup>/Vs is obtained with the mean value and standard deviation of  $141.6 \pm 11.5$  cm<sup>2</sup>/Vs, which is higher than that of ZnO-based TFTs<sup>3–20</sup> and even higher than that of a CVD-grown multilayered MoS<sub>2</sub> MOSFET<sup>21–24</sup>. To reach high mobility, epitaxial growth of crystalline MoS<sub>2</sub> on a crystal substrate is needed. Unfortunately, the mobility is lower for CVD-grown MoS<sub>2</sub><sup>25–28</sup> than peeled-off flakes from crystals<sup>21–28</sup>. The lattice mismatch caused defects are the other major concern for circuit yield. In contrast, high mobility SnO<sub>2</sub> TFT is achievable on the amorphous substrate



**Figure 3.** (a) DOS of (i) O, and (ii) Sn in SnO<sub>2</sub>, and (b) DOS of (i) O, and (ii) Zn in ZnO.

and free from lattice-mismatch defects. Such metal-oxide has already been used to manufacture TFT circuit for display. It is crucial to notice that the mobility of metal-oxide increases with increasing carrier density<sup>7</sup>. In the 4.5-nm-thick SnO<sub>2</sub> TFT, the high mobility is due to the high  $V_G$ -induced carrier density<sup>31</sup> of  $\sim 10^{13} \text{ cm}^{-2}$  to screen out charged defects. This is also supported by the higher mobility with larger  $V_G$ , where induced carrier density increases with  $V_G$ . In the thicker 7–20 nm SnO<sub>2</sub> devices with poor pinch off, the mobility is lowered by extra parallel conduction from non-depleted bulk SnO<sub>2</sub>. The mobility is lowered in 3.5 nm SnO<sub>2</sub> TFT due to stronger roughness scattering from top surface. Here the SnO<sub>2</sub> surface roughness is 0.39 nm, close to the HfO<sub>2</sub> roughness of 0.41 nm.

The high mobility SnO<sub>2</sub> TFT was further investigated using material analysis. Figure 2(a) shows the X-ray photoelectron spectroscopy (XPS) spectra from the Sn 3d and O 1s core level of the SnO<sub>2</sub> thin film. The Sn 3d peak corresponded to the oxidation state of Sn<sup>4+</sup>, and the O 1s peak was attributed to the O-Sn and O-H bonds. Thus, the chemical composition was determined to be Sn<sup>4+</sup>O<sub>2</sub><sup>2-</sup>. The X-ray diffraction spectroscopy (XRD) pattern in Fig. 2(b) reveals the presence of a rutile phase in SnO<sub>2</sub>. An average grain size of 7.9 nm was obtained using the Scherrer's equation. Figure 2(c) shows the cross-sectional transmission electron microscopy (TEM) image of the SnO<sub>2</sub>/HfO<sub>2</sub> stack. A relatively uniform SnO<sub>2</sub> layer with an ultra-thin thickness of 4.5 nm was observed.

To thoroughly understand the cause of the high mobility in SnO<sub>2</sub> TFT, first principle quantum-mechanical calculations were used to investigate the electronic structures of SnO<sub>2</sub> and ZnO; ZnO has been extensively studied using the localized density functional theory (DFT) to reveal the mechanism that leads to its high mobility. The structures of both SnO<sub>2</sub> and ZnO semiconductors were successfully obtained using local density approximation plus  $U$  (LDA+ $U$ ) method with appropriate  $U^p$  and  $U^d$  value. The LDA+ $U$  method compensates for the underestimation of the bandgap caused by a strong self-interaction by the DFT. The bandgaps of SnO<sub>2</sub> and ZnO were calculated to be 3.68 and 3.39 eV (Figure S1(a) and S1(b)), respectively, which are consistent with the experimental values of 3.6 and 3.4 eV, respectively. The contribution of each orbital in the conduction band minimum (CBM) of SnO<sub>2</sub> was investigated using density of state (DOS) analysis. The energy of valence band minimum was set to zero for convenience. As shown in Fig. 3(a), the utmost valence band was predominated by the O 2p orbitals, and the contribution from Sn was mostly from 5p orbitals. The lower conduction states near CBM were mostly derived from Sn 5s orbitals, whereas the O 2p orbitals contributed only in higher energy states. The Sn 4d orbitals did not give rise to the electron conducting property of SnO<sub>2</sub> because the antibonding interaction between Sn 4d and O 2p orbitals led only to the slight mixing of states at a deep valence band level. The DOS results of ZnO (Fig. 3(b)) were similar to those of SnO<sub>2</sub>. The major difference between the valence bands of SnO<sub>2</sub> and ZnO is the contribution of d orbitals. The upper valence bands (from -6 to 0 eV) were composed of primarily of O 2p orbitals and slight

mixing states from Zn 4s, 4p and 3d, whereas Zn 3d orbitals dominated in deeper states. In conduction band, Zn 4s was the major component near CBM while O 2p orbitals had little contribution at levels lower than 5 eV. Therefore, the high mobility of SnO<sub>2</sub> was attributed to the overlapping of s-orbitals, as with ZnO, although it had ns<sup>2</sup>np<sup>2</sup> configuration. This is further supported by the charge density distribution of SnO<sub>2</sub> shown in Figure S2(a), which has highly overlapped orbitals similar with those of ZnO in Figure S2(b). The highly overlapped orbitals of SnO<sub>2</sub> is related to large atomic radius, one row below Zn in the periodic table. From the results of DOS and charge density distribution, the higher mobility than the state-of-the-art ZnO TFTs<sup>32–33</sup> is attributed to the highly overlapped s-orbitals of SnO<sub>2</sub>.

The carrier effective mass is a major factor that may explain the higher mobility of SnO<sub>2</sub> than that of ZnO. The high electron mobility of n-type materials is caused by a deep curvature in CBM of band structure shown in Figure S1(a) and S1(b), which leads to a low effective mass of electrons. The calculated electron effective mass of SnO<sub>2</sub> was approximately 20% lighter than that of ZnO, indicating a faster electron transport in the SnO<sub>2</sub> conduction band.

In conclusion, this SnO<sub>2</sub> TFT device had a considerably high mobility, high  $I_{ON}/I_{OFF}$ , low SS, low operation voltage, and ultra-thin thickness. The low operation voltage is due to the high- $\kappa$  gate dielectric with a high capacitance density. The low SS indicates the good gate dielectric and SnO<sub>2</sub> interface. The high  $I_{ON}/I_{OFF}$  is related to the high mobility to increase  $I_{ON}$  and the ultra-thin thickness to decrease  $I_{OFF}$ , where the high mobility is caused by strongly overlapped s-orbitals.

## Methods

The SnO<sub>2</sub> TFTs were fabricated on a heavily doped n-type silicon (100) substrate. The 40-nm-thick high- $\kappa$  gate HfO<sub>2</sub> and 20–3.5-nm-thick SnO<sub>2</sub> films were deposited by physical vapor deposition. Thicker 20 nm SnO<sub>2</sub> film was also deposited for X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) pattern analysis. Then the high- $\kappa$  layer and SnO<sub>2</sub> film was annealed at 400°C. Finally, the Al source-drain electrodes were thermally evaporated and patterned. The gate length and width are 50–150  $\mu$ m and 500  $\mu$ m, respectively. Therefore, the maximum process temperature for this device is 400°C. The fabricated devices were characterized by XPS, XRD, TEM, C-V, and I-V measurements. All quantum-mechanical calculations were performed by Cambridge Sequential Total Energy Package (CASTEP) code. Structural optimization was performed on each model prior to calculating their electrical properties. The LDA+U method is known to correct the strong correlation of metal oxides and is proven to be quite effective for ZnO. The calculations were carried out by using generalized gradient approximation (GGA) with LDA+U.

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## Acknowledgements

This paper's publication was supported in part by Ministry of Science and Technology of Taiwan. We would like to thank the computing time support from National Taiwan University of Science & Technology and National Center for High-performance Computing.

## Author Contributions

C.W.S. did the experiments; A.C. supervised the experiments and wrote the main manuscript text; C.F.L. and W.F.S. did the quantum-mechanical calculations. All authors reviewed the manuscript.

## Additional Information

**Supplementary information** accompanies this paper at <http://www.nature.com/srep>

**Competing financial interests:** The authors declare no competing financial interests.

**How to cite this article:** Wei Shih, C. *et al.* Remarkably high mobility ultra-thin-film metal-oxide transistor with strongly overlapped orbitals. *Sci. Rep.* **6**, 19023; doi: 10.1038/srep19023 (2016).



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